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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/724,306	11/28/2000	Hua Zheng	1081	4823

7590 06/24/2005

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EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,306	ZHENG, HUA	
	Examiner	Art Unit	
	Man Phan	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34 and 36-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27 and 34* is/are allowed.

6)☒ Claim(s) *1-9,14-28,31-33 and 36-43* is/are rejected.

7)☒ Claim(s) *10-13,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Zheng for a "Data input and output circuits for multi-data rate operation" filed 11/28/2000 has been examined. Responsive to the restriction requirement filed on 11/30/2004, affirmation of the election has been made by applicant, and a provisional election was made with traverse to prosecute the invention of group I, claims 1-34 and 36-43. Claims 35 and 44-48 are withdrawn from further consideration by the Examiner, 37 C.F.R. ' 1.142(b), as being drawn to a non-elected invention. Claims 1-34 and 36-43 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molleron et al. (US#4,168,401) in view of Miyaou et al. (US#4,841,524).

With respect to claims 1, 2, 5, Molleron and Miyaou disclose a novel method and system for the data input and output in a multi data rate communications, according to the essential features of the claims. Mulleron et al. (US#4,168,401) discloses in Figs. 1 & 2 block diagrams

illustrated a digital switching unit for use in a multi rate time-division multiplex switching network wherein time-multiplexed data derived from time multiplexing of component data having different rates are interleaved with other time multiplexed data. All the incoming data transmitted on the lines T.sub.1 through T.sub.128 are time multiplexed by means of the multiplexer 1 shown in the Fig. 1, which converts them into parallel 8-bit words or octets with the cyclic rate of 1.024 megaoctet per second. A time base 3 in the digital switching unit receives a reference clock frequency at 2.048 MHz and provides all the signals of timing and addressing necessary to the digital switching unit. The timing signals thus deduced at 1.024 MHz, 64 kHz and 8 kHz are respectively the signal of second-order channel multiplexing, the bit clock signal and the octet clock signal for the second-order channels (*data bits received in a first order associated with time multiplexed data bits in a second order*) (Col. 2, lines 39 plus and Col. 5, lines 12 plus).

However, Molleron does not disclose expressly the associated output clock signal for the time multiplexed data bits in a second order. In the same field of endeavor, Miyaou et al. (US#4,841,524) discloses a digital data multiple conversion system, which can be used in a digital data communication network and recover lost clock pulses. The system includes a memory unit storing input data having N bits, a first frequency divider frequency-dividing an input clock having a first frequency at N to output a first frequency-divided signal, a first pulse width expansion circuit connected to receive m frequency divided pulses from the first frequency divider, where m indicates the number of lost pulses of the input clock plus one receiving the input clock, and outputting a first pulse width expanded signal of the input clock having an m+1 pulse width, a circuit outputting a read clock having a second frequency near to the the first

frequency and stuffing the read clock, a second frequency divider frequency-dividing the read clock at N to output a second frequency-divided signal, a second pulse width expansion circuit connected to receive n frequency divided pulses from the second frequency divider, where n indicates the number of lost pulses of the read clock plus one, receiving the read clock, and outputting a second width expanded signal of the read clock having an n+1 pulse width; a phase detector outputting a phase detection signal when the phases of both pulse width expanded signals coincide, and a stuffing request circuit outputting a stuffing request signal to the stuffing circuit. The stuffing circuit stuffs the read clock in response to the stuffing request signal (See Figs. 1 & 17; Col. 2, lines 31 plus).

One skilled in the art would have recognized the need for effectively and efficiently time multiplexing of component data having different rates and timing schemes, and would have applied Miyaou's teaching of the associated output clock signal for the time multiplexed data bits in a second order into Molleron's novel use of the digital switching unit in a multirate time division multiplex switching network. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Miyaou's digital data multiple conversion system for converting data having a frequency to data having another frequency by a digital stuffing method into Molleron's digital switching unit for a multirate TDM digital switching network with the motivation being to provide a method and system for a multi data rate operation.

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molleron et al. (US#4,168,401) in view of Miyaou et al. (US#4,841,524) as applied to the claims above, and further in view of Kato et al. (US#5,995,441).

With respect to claims 3 and 4, Molleron and Miyaou disclose the claimed limitations discussed in paragraph 3 above. However, these claims differ from the claims above in that the claims require for a delay lock loop circuit configured to provide a particular delay for the output clock signal. In the same field of endeavor, Kato et al. (US#5,995,441) provides a synchronous semiconductor memory device synchronized with an external clock signal to receive an address signal and a control signal, in which a delay locked loop circuit configured of the variable delay circuit, a phase comparator circuit, a shift logic circuit, a delay control data holding circuit, a variable constant current circuit and a voltage generating circuit controls phasing of internal and external clock signals (See Fig. 3; Col. 4, lines 15 plus).

One skilled in the art would have recognized the need for effectively and efficiently time multiplexing of component data having different rates and timing schemes, and would have applied Kato's delay locked loop circuit for the variable delay and Miyaou's teaching of the associated output clock signal for the time multiplexed data bits in a second order into Molleron's novel use of the digital switching unit in a multirate time division multiplex switching network. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Kato's synchronous semiconductor memory device capable of rapidly, highly precisely matching internal clock phase to external clock phase, and Miyaou's digital data multiple conversion system for converting data having a frequency to data having another frequency by a digital stuffing method into Molleron's digital switching unit for a multirate TDM digital switching network with the motivation being to provide a method and system for a multi data rate operation.

5. Claims 6-9, 14-26 and 28,31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molleron et al. (US#4,168,401) in view of Kato et al. (US#5,995,441).

With respect to claims 6-9, 14-26 and 28,31-33, Molleron and Kato disclose a novel method and system for the data input and output in a multi data rate communications, according to the essential features of the claims. Mulleron et al. (US#4,168,401) discloses in Figs. 1 & 2 block diagrams illustrated a digital switching unit for use in a multi rate time-division multiplex switching network wherein time-multiplexed data derived from time multiplexing of component data having different rates are interleaved with other time multiplexed data. All the incoming data transmitted on the lines T.sub.1 through T.sub.128 are time multiplexed by means of the multiplexer 1 shown in the Fig. 1, which converts them into parallel 8-bit words or octets with the cyclic rate of 1.024 megaoctet per second. A time base 3 in the digital switching unit receives a reference clock frequency at 2.048 MHz and provides all the signals of timing and addressing necessary to the digital switching unit. The timing signals thus deduced at 1.024 MHz, 64 kHz and 8 kHz are respectively the signal of second-order channel multiplexing, the bit clock signal and the octet clock signal for the second-order channels (*data bits received in a first order associated with time multiplexed data bits in a second order*) (Col. 2, lines 39 plus and Col. 5, lines 12 plus).

However, Molleron does not disclose expressly the associated data latches coupled to the first multiplexer and configured to receive and latch the set of data bits in the second order to provide a set of latched data bits. In the same field of endeavor, Kato et al. (US#5,995,441) provides a synchronous semiconductor memory device synchronized with an external clock signal to receive an address signal and a control signal, in which a delay locked loop circuit

configured of the variable delay circuit, a phase comparator circuit, a shift logic circuit, a delay control data holding circuit, a variable constant current circuit and a voltage generating circuit controls phasing of internal and external clock signals (See Fig. 3; Col. 4, lines 15 plus). Kato further teach in Fig. 1 a block diagram illustrated a synchronous semiconductor memory device 1000 includes: a control circuit 20 receiving an external clock signal Ext.CLK and external control signals /RAS, /CAS, /W, /CS and the like applied via a group of external control signal input terminals 10 to produce an internal control signal; and a memory cell array 100 having memory cells arranged in a matrix. Synchronous semiconductor memory device 1000 also includes: a row predecoder 36 provided for each pair of memory cell blocks and controlled by control circuit 20 to latch and predecode a row address transmitted on address bus 50c; a row decoder 44 selecting a corresponding row (i.e. a word line) of a memory cell block that is selected based on an output from row predecoder 36; a predecoder 34 provided for each memory cell block and controlled by control circuit 20 to latch and predecode a column address transmitted on address bus 50c; a column predecoder 40 further predecoding a column address according to an output from predecoder 34; and a column decoder 42 selecting a corresponding column (i.e. a pair of bit lines) of a memory cell block that is selected based on an output from column predecoder 40 (Col. 6, lines 15 plus).

Regarding claims 36-43, they are method claims corresponding to the apparatus claims 6-9, 14-26 and 28, 31-33 above. Therefore, claims 36-43 are analyzed and rejected as previously discussed with respect to claims 6-9, 14-26 and 28,31-33.

One skilled in the art would have recognized the need for effectively and efficiently time multiplexing of component data having different rates and timing schemes, and would have

applied Kato's delay locked loop circuit for the variable delay into Molleron's novel use of the digital switching unit in a multirate time division multiplex switching network. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Kato's synchronous semiconductor memory device capable of rapidly, highly precisely matching internal clock phase to external clock phase into Molleron's digital switching unit for a multirate TDM digital switching network with the motivation being to provide a method and system for a multi data rate operation.

Allowable Subject Matter

6. Claims 27 and 34 are allowable.

Claims 10-13 and 29-30 are objected to as being dependent upon the rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

7. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein a second multiplexer coupled to the data latches and configured to receive and multiplex the set of latches data bits to provide time multiplexed data bits, and wherein the at least one output driver is configured to receive and provide signal drive for the time multiplexed data bits, as specifically recited in claims 10-13; wherein the sequence of time multiplexed data bits includes two data bits per active cycle of an input clock signal, and wherein the plurality of sequences of data bits include a

first sequence and a second sequence, the first sequence including data bits corresponding a first phase of the input clock signal and the second sequence including data bits corresponding to a second phase of the input clock signal, as specifically recited in claims 29-30.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Zheng et al. (US#5,805,505) is cited to show the circuit and method for converting a pair of input signals into a level limited output signal.

The Zheng (US#6,157,560) is cited to show the memory array datapath architecture.

The Zheng et al. (US#6,480,428) is cited to show the redundant circuit for memory.

The Zheng (US#6,094,396) is cited to show the memory array architecture for multi data rate operation.

The Chapman et al. (US#5,684,421) is cited to show the compensated del;ay locked loop timing vernier.

The Foss et al. (US#6,314,052) is cited to show the delayed locked loop implementation in a synchronous dynamic random access memory.

The Choudlhury (US#6,229,367) is cited to show the method and apparatus for generating a time delayed signal with a minimum data dependency error using an oscillator.

The Lee (US#6,282,128) is cited to show the integrated circuit memory devices having multiple data rate mode capability and methods of operating same.

The Ellis et al. (US#6,539,064) is cited to show the multiple data rate filtered modulation system for digital data.

The Texier et al. (US#3,987,251) is cited to show the time division switching network for switching multirate multiplexed data.

The Goto et al. (US#5,280,195) is cited to show the timing generator.

The Box et al. (US#4,908,784) is cited to show the method and apparatus for asynchronous time measurement.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Man U. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached Monday through Friday from 6:00 am to 3:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at toll free 1-866-217-9197.

MPhan

06/22/2005

MAN U. PHAN
PRIMARY EXAMINER